Remarks/Arguments

Applicants have received the Office Action dated August 11, 2008, in which the Examiner: 1) rejected claims 1, 2, 7-12, 25, and 25-28 under 35 U.S.C. § 103(a) as allegedly obvious over Chennupaty (U.S. Patent No. 6,014,735) in view of Narayan (U.S. Patent No. 6,161,172) and in further view of Leijten (U.S. Patent Publication No. 2002/0116598); 2) rejected claims 3, 4, 13, 15, 16, and 27 as allegedly obvious over Chennupaty in view of Narayan and further in view of Leijten and Google (New bytecodes for "real" Java?); 3) rejected claims 5, 6, 14 and 26 as allegedly obvious over Chennupaty, Narayan, Leijten and JVM (The JavaTM Virtual Machine Specification); and 4) rejected claims 17-20, and 23-24 as obvious over Chennupaty in view of Narayan and further in view of Leijten and Nazomi (First Universal Java Accelerator Chip for Mobile Wireless Applications). Based on the arguments herein, Applicants respectfully submit that all pending claims are in condition for allowance.

Independent claim 1 requires "the decode logic causes a program counter to skip the prefix thereby precluding the decode logic from receiving the prefix." The Examiner admits that Chennupaty and Narayan fail to teach this limitation,[1] and instead the Examiner turns to Leijten. Specifically, the Examiner asserts that paragraph 17 of Leijten discloses "incrementing a program counter to skip bytes that should not be executed/decoded." Office Action, p. 4.

Respectfully, the Examiner's argument regarding Leijten is mistaken. Contrary to the Examiner's assertion, Leijten does **not** disclose incrementing a program counter to skip bytes that should not be decoded. Instead, paragraph 17 of Leijten teaches that a current instruction in a current memory line signals whether the program counter has to "skip padding" in a remaining part of the current memory line to advance to a start of the subsequent memory line. Stated in another way, Leijten teaches that when dealing with a

[1] The Examiner does assert, however, that Chennupaty discloses precluding the decode logic from receiving the prefix at fig. 4, ref. 420 and EN1, and col. 5, ll. 59-65.

particular memory line, a current instruction in that line can cause the program counter to skip padding in another part of that memory line, such that the next memory line is processed. However, Leijten does not teach or even suggest that such skipping prevents decoding of the remainder of the memory line; it only teaches that such skipping prevents execution of the remainder of the memory line. In fact, given that entire memory lines are fetched at a time (para. 16, lines 3 and 5-6), and further given that the instruction that causes the skipping has already been decoded and executed, it is quite likely that the part of the memory line that is skipped has already been decoded and is ready for execution. Thus, because Leijten does not teach that its skipping prevents decoding (as required by claim 1), and further because Leijten actually suggests that decoding of the skipped portion has already taken place, the Examiner is mistaken when he states that Leijten teaches incrementing a program counter that prevents a decode logic from receiving a byte or prefix.

In making his obviousness rejection, the Examiner apparently used Leijten to connect the concept of using a program counter for preventing decode of bytes to the concept of precluding decode logic from receiving a prefix as allegedly disclosed in Chennupaty. However, respectfully, Applicants' argument above nullifies the Examiner's assertions regarding Leijten. Thus, no art of record introduces the concept of using a program counter to prevent prefixes from being decoded. Absent such teaching, the combination of Chennupaty, Narayan and Leijten fails to render claim 1 obvious. Further, no other art of record satisfies the deficiencies of Chennupaty, Narayan and Leijten. Thus, claim 1 and the claims dependent upon claim 1 are patentable over all possible combinations of the art of record.

Independent claim 9 requires "if the subsequent instruction includes the predetermined prefix, causing a program counter to skip the predetermined prefix to thereby preclude decode logic from receiving the prefix and changing the decoding of the subsequent instruction according to a second behavior." As explained above with reference to claim 1, no combination of the art of record teaches or suggests such a

limitation. Thus, claim 9 and all claims dependent upon claim 9 are patentable over all combinations of the art of record.

Independent claim 17 requires "pre-decode logic determining if a subsequent instruction comprises a prefix in which case a program counter skips the prefix thereby precluding the decode logic from receiving the prefix." As explained above, no combination of the art of record teaches or suggests such a limitation. Thus, claim 17 and all claims dependent on claim 17 are patentable over all combinations of the art of record.

Independent claim 25 requires "wherein if the subsequent instruction comprises the prefix, the register skips the prefix of the subsequent instruction thereby precluding the decode logic from receiving the prefix." As explained above, no combination of the art of record teaches or suggests such a limitation. Thus, claim 25 and all claims dependent on claim 25 are patentable over all combinations of the art of record.

Conclusion

Applicants respectfully request reconsideration and that a timely Notice of Allowance be issued in this case. In the event that an extension of time is necessary to allow for consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required (including fees for net addition of claims) are hereby authorized to be charged to Texas Instruments Incorporated's Deposit Account No. 20-0668 for such fees.

Respectfully submitted,

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